ShriPhanishwarNathRenu Engineering College, Araria

(Under Department of Science & Technology and Technical Education Patna, Govt. of Bihar)

Ref. No: SPNREC/322 Date: 08-03-2025

Room No: 06

Time Table, SPNREC ARARIA

W.E. F: - 08-03-2025

5TH SEMESTER ,ECE

	Period 1	Period 2	Period 3		Period 4	Period 5	Period 6
Day	**10:00–11:00**	**11.00–12.00**	**12:00–1:00**	**1:00-2:00**	**2:00-3:00**	**3:00-4:00**	**4.00-5:00**
Mon	Computer Network & Security	Linear Control System	Digital Signal Processing	LUNCH BREAK	Digital Signal Processing Lab		Library
Tue	Probability & Stochastic Processes	Linear Control System	Linear Integrated Circuit		- Library --	Library	
Wed	Computer Network & Security	Linear Integrated Circuit	Linear Control System		Microprocessor & Microcontroller Lab		Library
Thu	Microprocessor & Microcontroller	Computer Network & Security	Digital Signal Processing		- Library --	Library	
Fri	Microprocessor & Microcontroller	Probability & Stochastic Processes ---	Linear Integrated Circuit		Linear Integrated Circuit Lab ---		Library
Sat	Microprocessor & Microcontroller	Probability & Stochastic Processes	Digital Signal Processing		Summer Enterpreneurship II		Library

Course Title	Faculty Name
Digital Signal Processing (T+P)	Prof. Priyatam Kumar, Asst Prof. ECE
Linear Integrated Circuit (T+P)	Prof. Amit Ranjan, Asst Prof. ECE
Microprocessor & Microcontroller(T+P)	Prof. Shaheen, Asst Prof. ECE
Linear Control System	Prof. Dharmendra Kumar, Assistant Prof., ECE
Probability & Stochastic Processes	.Dr. Ritesh Kumar, Assistant Prof. ECE
Computer Network & Security	Prof. Abnish Ranjan,Assistant Prof. CSE
Summer Enterpreneurship II	Prof. Priyatam Kumar, Asst Prof. ECE

Professor I/C Time Table(ECE) 08/03/25

HOD(ECE) 08/03/25

Professor I/C Time Table 08/03/2025

Dean (Academic) 08/03/25

Principal 08-03-25

SPNREC, ARARIA